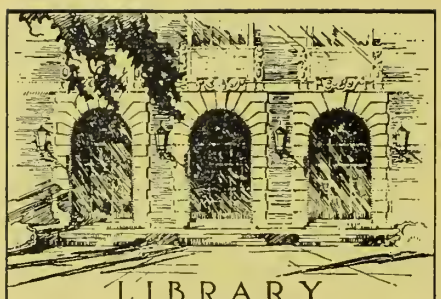
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Report No. 202

JUL 28 1966

MULTIVIBRATOR TRIGGERING REQUIREMENTS

by

Walter John Wattman

April 15, 1966

JUL 7 1966

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MULTIVIBRATOR TRIGGERING REQUIREMENTS*

by

Walter John Wattman

April 15, 1966

Department of Computer Science
University of Illinois
Urbana, Illinois

* This work was submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering, April, 1966.

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1. INTRODUCTION

The basic concept in switching circuitry is that of a discrete change of state. Two states are considered in transistor switching circuitry, the ON state and the OFF state. In saturated switching circuits, the ON state is marked by a very low collector to emitter voltage and a relatively large collector current, while the OFF state is marked by a relatively high collector to emitter voltage and a very small collector current.

The selection of component values and supply voltages which allow this change of state is called the "dc design procedure." The dc design procedure may also provide for the optimization of the circuit with respect to such quantities as available output power and power drain. A worst case design analysis is one which takes into account the maximum variation of each supply voltage and component value. Each performance property (cut-off voltage, required H_{FE}, etc.) is examined in turn, assuming that in each case the most unfavorable combination of tolerance swings for that property will occur. The sensitivity of circuit performance to normal variations in transistor and component parameters makes the use of such an analysis mandatory if reliable circuits are to be designed.

Worst case dc design procedures do not always guarantee proper transient operation of a bistable circuit. In order for the circuit to be useful the designer must be able to reliably predict conditions which are sufficient to cause a state transition. That is, the designer needs the capability of specifying the characteristics of those triggering signals which will always cause transition and of those which will never cause transition. The problem may be further complicated by the requirement that the transition occur within a specified time interval.

The object of this investigation is to provide a scheme for the worst case analysis of the triggering requirements of saturated transistor circuitry. The circuit configuration to be considered is that of a standard bistable multivibrator, or flipflop, employing base triggering of the ON transistor. The treatment is divided into three parts: slow dc coupled triggering, fast dc coupled triggering, and fast ac coupled triggering. Conclusions reached in the third part apply equally well to a monostable, or one-shot, multivibrator.

2. SLOW DC TRIGGERING

When triggering a multivibrator with a dc coupled step, AU(t), there is only one question which needs to be answered. Namely: how large must the magnitude of A be to insure that a state transition occur?

Figure 2.1 is the circuit of a flipflop which has been simplified by removing the trigger steering networks and the speed-up capacitors in the base-collector coupling networks. During transition this circuit is unstable, a condition which exists until currents are limited by the non-linearities of the transistor saturation and/or cut-off. The circuit requirements sufficient to sustain this instability may be placed in evidence in the following manner. Assume that at time t, $t < 0$, Q_1 is ON. Apply a voltage step AU(t) to terminal T of Figure 2.1, where A is large enough to cause transition. Then for $t > 0$, but before limiting takes place, both Q_1 and Q_2 are active. During this instability the volt-ampere charactistics which the circuit presents to the coupling resistor, R_7, must represent a negative resistance. Referring to Figure 2.2, let Q_1 and Q_2 have common emitter forward current transfer ratios of H_{FE1} and H_{FE2} respectively. The node equation representation of the circuit of Figure 2.2 is

$$H_{FE1} I_{b1} = \frac{V_2 - V_{cc}}{R_6} - i \qquad 2.1$$

$$H_{FE2} I_{b2} = \frac{V_4 - V_{cc}}{R_2} + \frac{V_4 - V_1}{R_3} \qquad 2.2$$

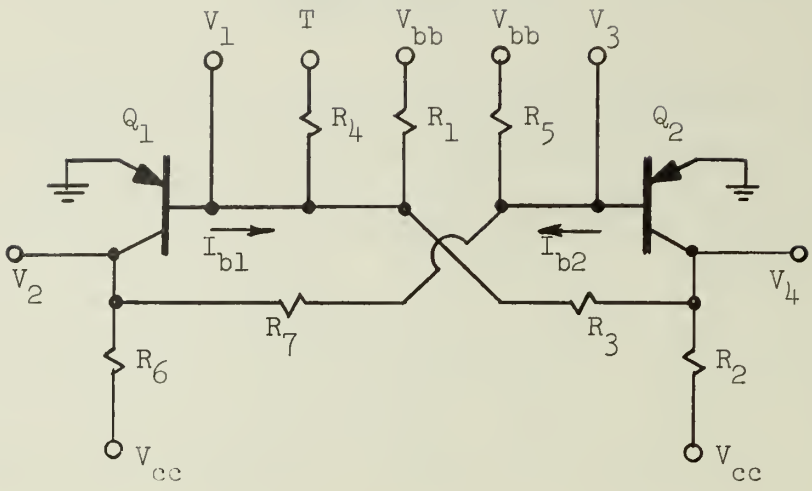

Figure 2.1 Multivibrator Circuit.

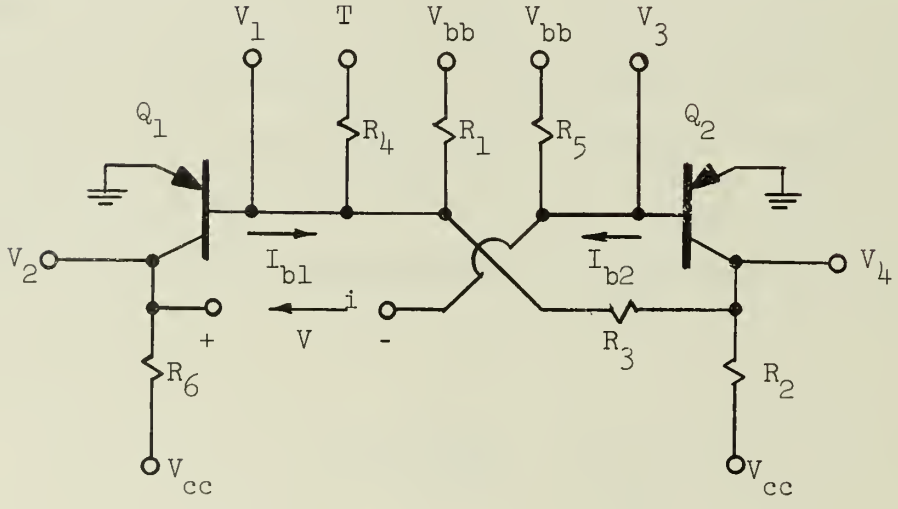

Figure 2.2 Circuit for Calculation of dv/di

$$I_{b1} + \frac{A - V_1}{R_4} + \frac{V_{bb} - V_1}{R_1} = \frac{V_1 - V_4}{R_3} \qquad 2.3$$

$$I_{b2} + \frac{V_{bb} - V_3}{R_5} = i \qquad 2.4$$

$$V_2 = V_3 + v \qquad 2.5$$

Noting that V_1 and V_3 are constant (because of forward biased base-emitter junctions), taking differentials, and solving for the resistance characteristic gives

$$\frac{dv}{di} = R_6 \left[1 - \frac{H_{FE1} \; H_{FE2}}{\frac{R_3}{R_2} + 1} \right] \qquad 2.6$$

which when combined with the restraint for negative resistance

$$\frac{dv}{di} < 0 \qquad 2.7$$

gives

$$H_{FE1} \; H_{FE2} > \frac{R_3}{R_2} + 1 \qquad 2.8$$

as a condition for instability. With the result of Eq. 2.8 it is worthwhile to examine the transition process more carefully. For discussion purposes let a ramp voltage

$$B(t) = btU(t) \tag{2.9}$$

where b is small, be applied to terminal T of Figure 2.1. At time t, $t < 0$, let Q_1 be ON and Q_2 be OFF. The following terms may be defined:

I_{blq} = the quiescent base current, $t < 0$

I_{blsat} = the base current which will just cause saturation

I_{clq} = the quiescent collector current, $t < 0$

$I_t(t)$ = the trigger current

where

$$I_{blsat} = \frac{I_{clq}}{H_{FE1}} \tag{2.10}$$

and in general

$$I_{blq} > I_{blsat} \tag{2.11}$$

Voltage V_1 is held constant by the forward biased base-emitter junction of Q_1 and since Q_2 is cut off it follows that

$$I_{R3} = \frac{V_1 - V_{cc}}{R_3 + R_2} = \text{constant} \tag{2.12}$$

$$I_{R1} = \frac{V_{bb} - V_1}{R_1} = \text{constant} \tag{2.13}$$

$$I_{bl}(t) = I_{blq} - \frac{btU(t) - V_1}{R_4} \qquad 2.14$$

$I_{bl}(t)$ is decreasing with time, therefore there exists some time t_1, $t_1 > 0$, such that

$$I_{bl}(t_1) = I_{blsat} \qquad 2.15$$

For time greater than t_1, $I_{bl}(t)$ is no longer great enough to maintain Q_1 in saturation and hence $I_{cl}(t)$ becomes a function of $I_{bl}(t)$

$$I_{cl}(t) = H_{FE1}\, I_{bl}(t), \quad t > t_1 \qquad 2.16$$

Voltages $V_2(t)$ and $V_3(t)$ are given by

$$V_2(t) = \frac{R_6\, I_{cl}(t) + \frac{R_6\, V_{bb}}{R_5 + R_7} + V_{cc}}{1 - \frac{R_6}{R_5 + R_7}}, \quad t > t_1 \qquad 2.17$$

$$V_3(t) = \frac{V_{bb}\, R_7 + V_2(t)\, R_5}{R_5 + R_7}, \quad t > t_1 \qquad 2.18$$

and are also decreasing functions of time. There exists some time t_2, $t_2 > t_1$, such that $V_3(t_2)$ will be low enough to forward bias the base-emitter junction of Q_2. This occurs when

$$V_3(t_2) = V_{BE2ON} \qquad 2.19$$

Since $t_2 > t_1$, Q_1 is in its linear range and H_{FE1} is high, say

$$H_{FE1} > 10 \tag{2.20}$$

For practical circuits

$$\frac{R_3}{R_2} < 19 \tag{2.21}$$

and hence Eq. 2.8 implies that a sufficient condition to insure regeneration is

$$H_{FE2} > 2 \tag{2.22}$$

In practice this condition is met at virtually the time when Q_2 starts to conduct. Making use of Eqs. 2.9, 2.14, and 2.16, the voltage at the trigger point at time t_2 can be expressed as:

$$B(t_2) = R_4 I_{blq} - \frac{R_4}{H_{FE1}} I_{c1}(t_2) + V_1 \tag{2.23}$$

The current delivered by the trigger source at time t_2 is

$$I_t(t_2) = \frac{B(t_2) - V_1}{R_4} = I_{blq} - \frac{I_{c1}(t_2)}{H_{FE1}} \tag{2.24}$$

Reasonable circuit design demands that $I_{c1}(t_2)$ be less than the saturation value, but somewhat greater than zero, or:

$$I_{clq} > I_{c1}(t_2) > 0 \tag{2.25}$$

By making use of Eqs. 2.17, 2.18, and 2.19, $I_{c1}(t_2)$ can be expressed as

$$I_{c1}(t_2) = V_{BE2on}\left[\frac{R_5+R_6+R_7}{R_5R_6}\right] - V_{bb}\left[\frac{R_6+R_7}{R_5R_6}\right] - \frac{V_{cc}}{R_6} \qquad 2.26$$

Aside from the value of V_{BE2on}, which changes little from one transistor to another, the value of $I_{c1}(t_2)$ is controlled by the circuit design, i.e., the proper choice of R_5, R_6, R_7, V_{bb}, and V_{cc}.

Equations 2.24 and 2.25 indicate that the required trigger current is less than the quiescent base current, the difference being the quantity $I_{c1}(t_2)/H_{FE1}$. Equation 2.26 shows that $I_{c1}(t_2)$ is fixed by external circuitry, but the influence of H_{FE1} is imposed by the transistor. For very large H_{FE1},

$$\lim_{H_{FE1}\to\infty} I_t = I_{blq} \qquad 2.27$$

and it can be concluded that as H_{FE1} increases, the required trigger current increases, but that it is bounded by an upper limit, the quiescent base current.

3. FAST DC TRIGGERING

It has been shown in Part 2 of this report that a trigger current pulse with a magnitude equal to the magnitude of the quiescent base current is sufficient to insure a state transition in the circuit configuration detailed in Figure 2.1. However, this does not convey any information about the propagation time of the pulse through the circuit. That is, the circuit does not switch in zero time after the trigger exceeds the threshold level.

Referring to Figure 3.1, the following terms are defined:

T_s = storage time, the elapsed time between the application of $I_t U(t)$ and a ten per cent change in the collector voltage, V_1 (seconds $\times 10^{-6}$)

T_t = transition time, the elapsed time between a ten per cent change and a 90 per cent change in the collector voltage, V_1 (seconds $\times 10^{-6}$)

I_{bq} = quiescent base current, $t < 0$ (amperes $\times 10^{-3}$)

I_{cq} = quiescent collector current, $t < 0$ (amperes $\times 10^{-3}$)

P = normalized trigger current (amperes $\times 10^{-3}$)

$C(T_s)$ = normalized charge, the charge necessary to cause a ten per cent change in the collector voltage, V_1, at time $t = T_s$ (coulombs $\times 10^{-9}$)

where the following relations hold

$$P = \frac{I_t}{|I_{bq}|} \qquad 3.1$$

$$C(T_s) = \int_0^{T_s} P\, dy = P\, T_s \qquad 3.2$$

A group of transistors was selected for high and low H_{FE} from several different lots totaling a few hundred.* Thus in one sense the components represented the best and the worst of a particular type. The circuit of Figure 3.1 was used and the following data was taken in an attempt to place in evidence the factors which determine T_s. Figure 3.2 is a plot of $C(T_s)$ with I_{cq}, I_{bq}, and V_{cc} held constant, for the best transistor, TR_1, and the worst transistor, TR_2. The C characteristics of the remaining transistors fell between those of TR_1 and TR_2.

From Eq. 3.2 it is seen that in general

$$P = \frac{C(T_s)}{T_s} \qquad 3.3$$

and that curves of constant P in Figure 3.2 will be straight lines passing through the origin with slope P. The value of P for any of these lines can be read directly by noting that at $T_s = 1$, $P = C(1)$. The intersection of a line of constant P and the C characteristic of a particular transistor yields the storage time of that transistor for that value of P. It is clear that as P approaches unity, the intersection becomes less well defined and T_s increases greatly.

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* 2N3638's manufactured by Fairchild.

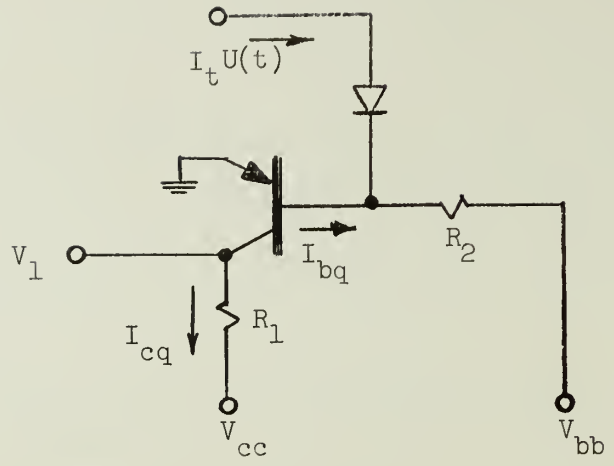

Figure 3.1 Test Circuit for $C(T_s)$

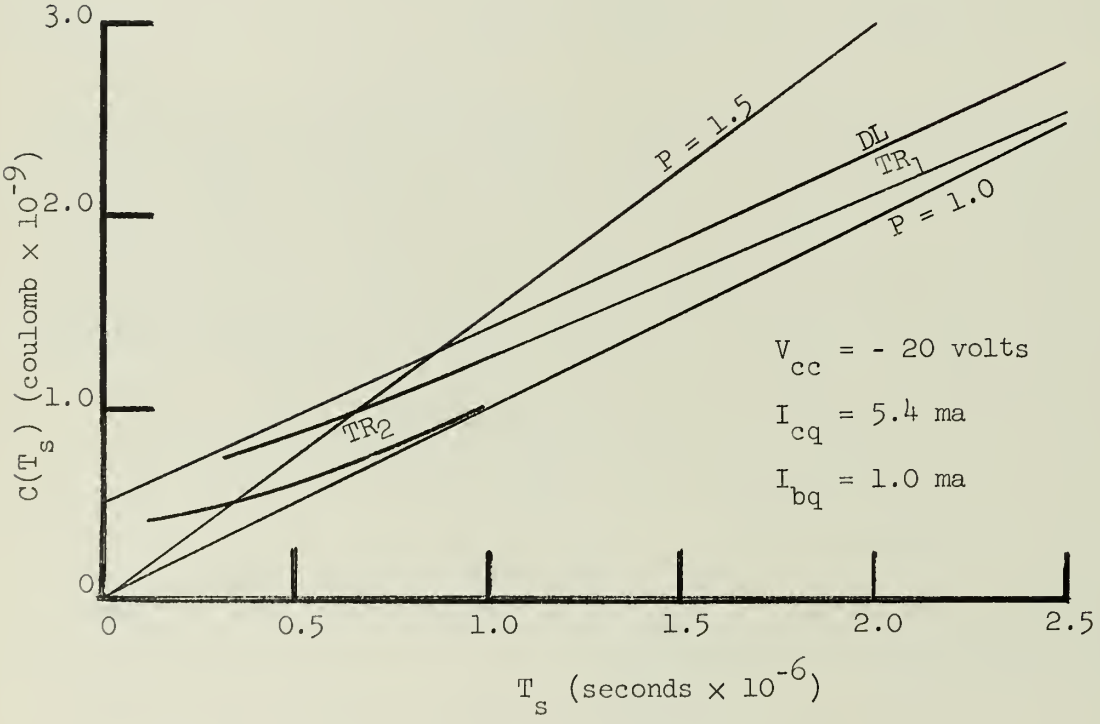

Figure 3.2 C Characteristics for TR_1 and TR_2.

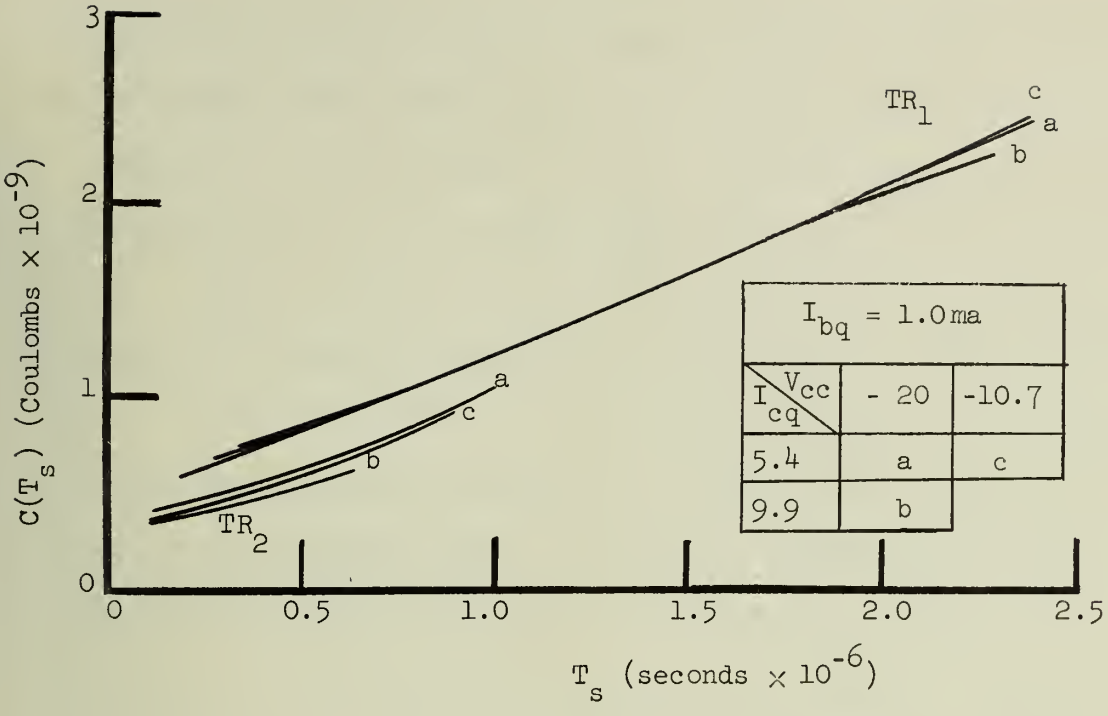

Figure 3.3 C Characteristic Variations

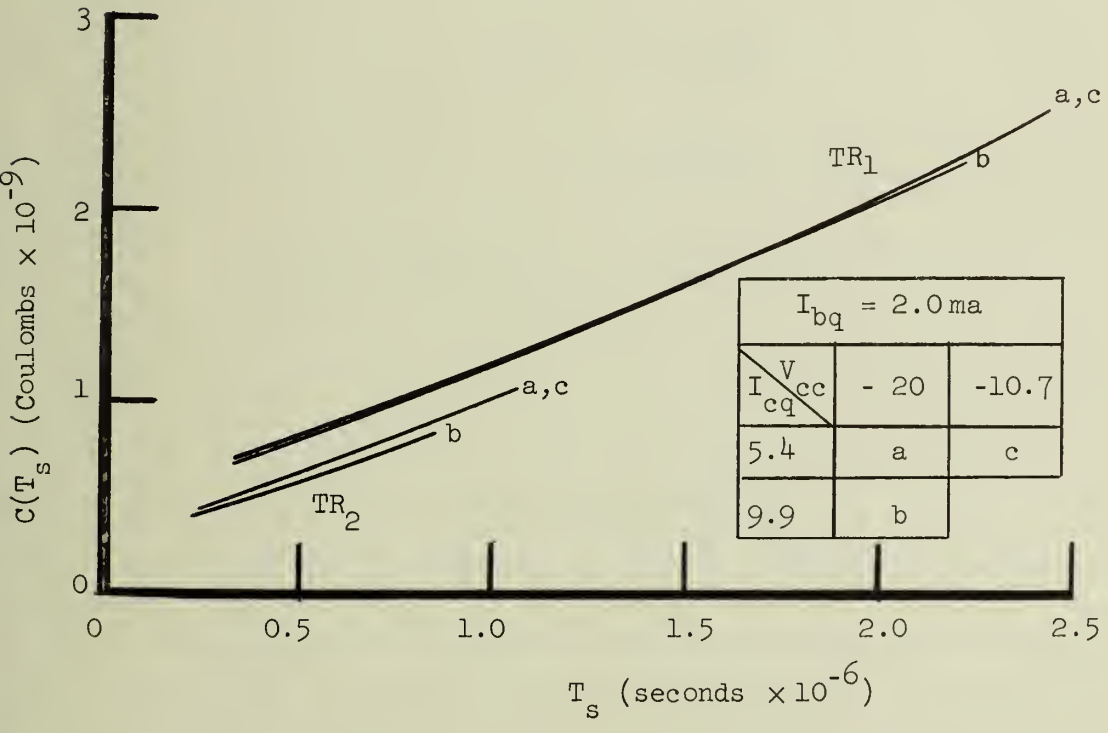

Figure 3.4 C Characteristic Variations

The variation of the C characteristics as a function of V_{cc}, I_{cq}, and I_{bq} was investigated and the data is summarized in Figures 3.3 and 3.4. These figures indicate that the C characteristic of a given transistor is relatively constant with respect to a two-to-one change in V_{cc}, I_{cq}, or I_{bq}. Relatively constant is taken to mean that the described variation is less than the variation occuring within a population of transistors as displayed in Figure 3.2.

In view of the supporting information indicating that the C characteristics are constant over some specified operating range it is reasonable to return to Figure 3.2 and establish a design line, DL, which will be taken to represent the worst case transistor over the operating range. Choosing the design line to be linear in T_s, it must satisfy the equation

$$C(T_s) = a + b\,T_s \tag{3.4}$$

where for the design line in Figure 3.2

$$a = 0.5 \times 10^{-9} \text{ coulomb}; \quad b = 0.9 \times 10^{-3} \text{ amperes}. \tag{3.5}$$

Combining Eq. 3.2 and 3.4 gives

$$\int_0^{T_s} P\,dy = a + b\,T_s \tag{3.6}$$

Performing the integration and solving for P as a function of T_s yields the worst case value of P, P_{min}.

$$P_{min} = \frac{a}{T_s} + b \qquad 3.7$$

Figure 3.5 is a plot of equation 3.7. Since switching will always occur for $P > 1$, as shown in Part 2, the curves of Figure 3.5 can be used to find the value of P required to guarantee that the storage time does not exceed some maximum value, T_s. An order of magnitude estimate for the transition time, T_t, is

$$T_t \cong T_s. \qquad 3.8$$

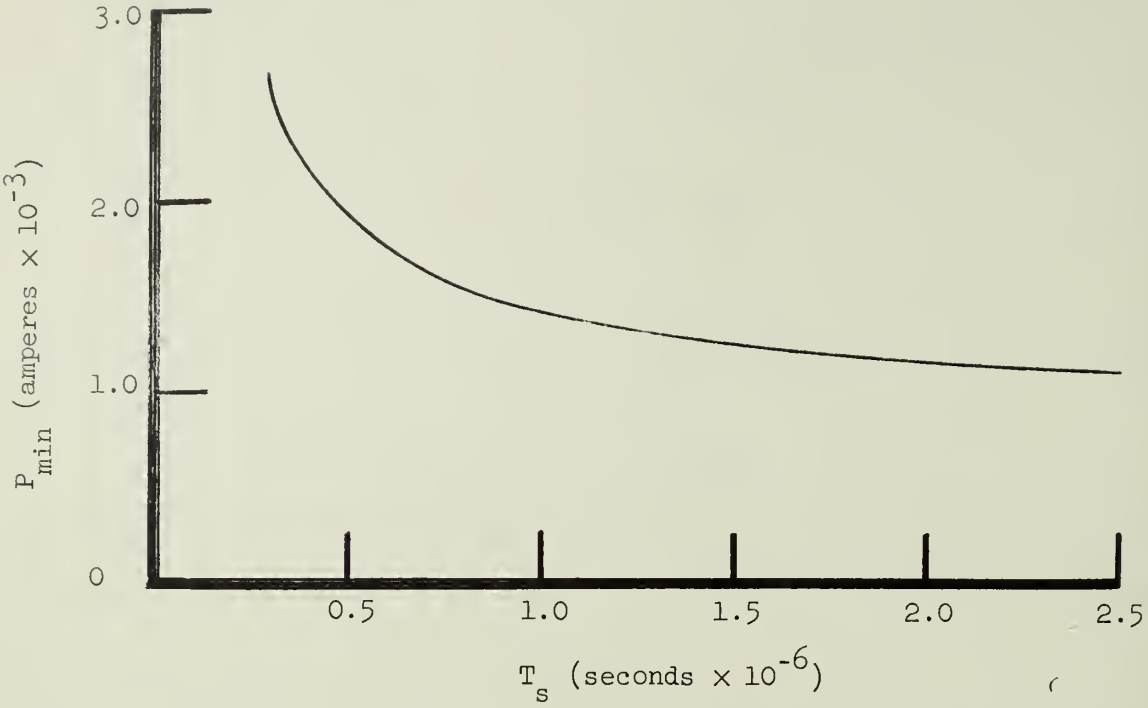

Figure 3.5 P_{min} as a Function of T_s.

When the transistor of Figure 3.1 is cross-coupled with another in a bistable circuit, regeneration may cause T_t to drop to as little as 0.2 T_s.

4. FAST AC TRIGGERING

The results of Part 3 of this presentation can be extended to those cases where the trigger current is not a step function. In particular, suppose the normalized trigger pulse has the form

$$I_t(t) = P \exp(-gt)\, U(t) \tag{4.1}$$

which commonly results from capacitor coupling between the trigger and the circuit to be triggered. Eq. 3.2 then has the form

$$C(T_s) = \int_0^{T_s} P \exp(-gy)dy \tag{4.2}$$

and the result of combining this with the design line Eq., 3.4, is

$$\int_0^{T_s} P \exp(-gy)dy = a + b\, T_s \tag{4.3}$$

which when integrated gives P as a function of T_s and g.

$$P = \frac{g\, a + b\, T_s}{1 - \exp(-gT_s)} \tag{4.4}$$

In the limit as g approaches zero, Eq. 4.4 reduces to Eq. 3.7. Figure 4.1 displays P plotted as a function of T_s with g as a parameter. Figure 4.2 presents data which justifies this extension to nonrectangular waveforms. The actual C characteristics for TR_1 and TR_2 which were determined in Part 3 are compared with data points taken for various exponential waveforms.

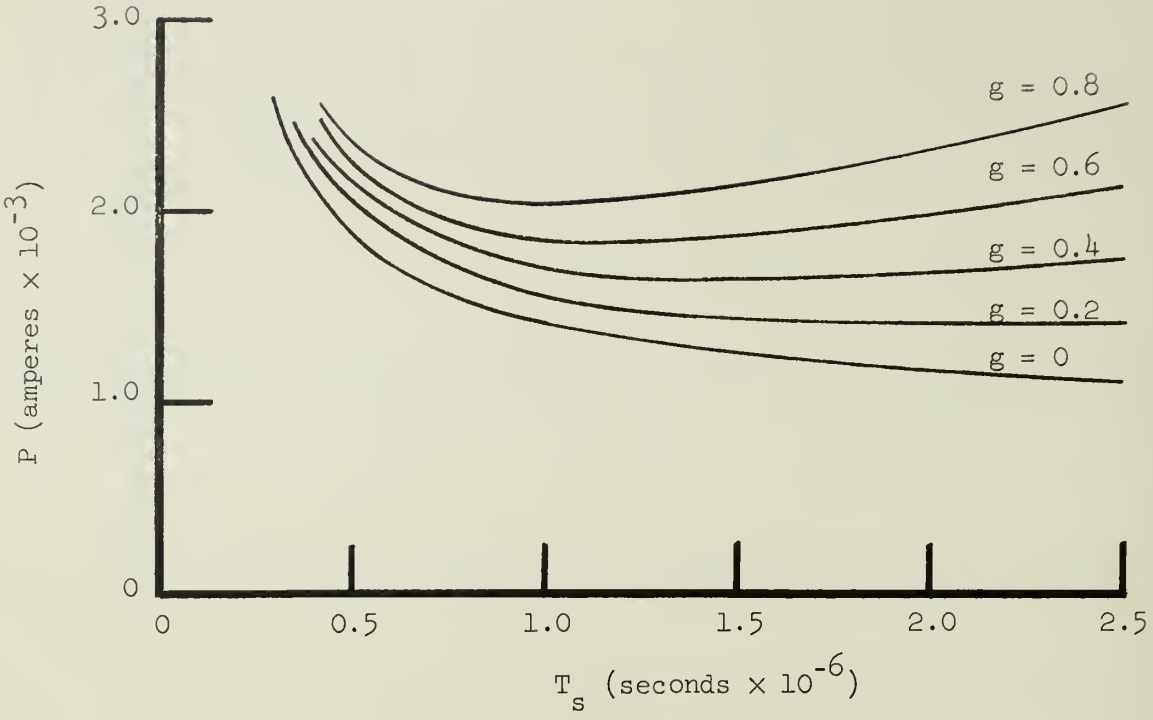

Figure 4.1 Normalized Trigger Current as a Function of T_s and g.

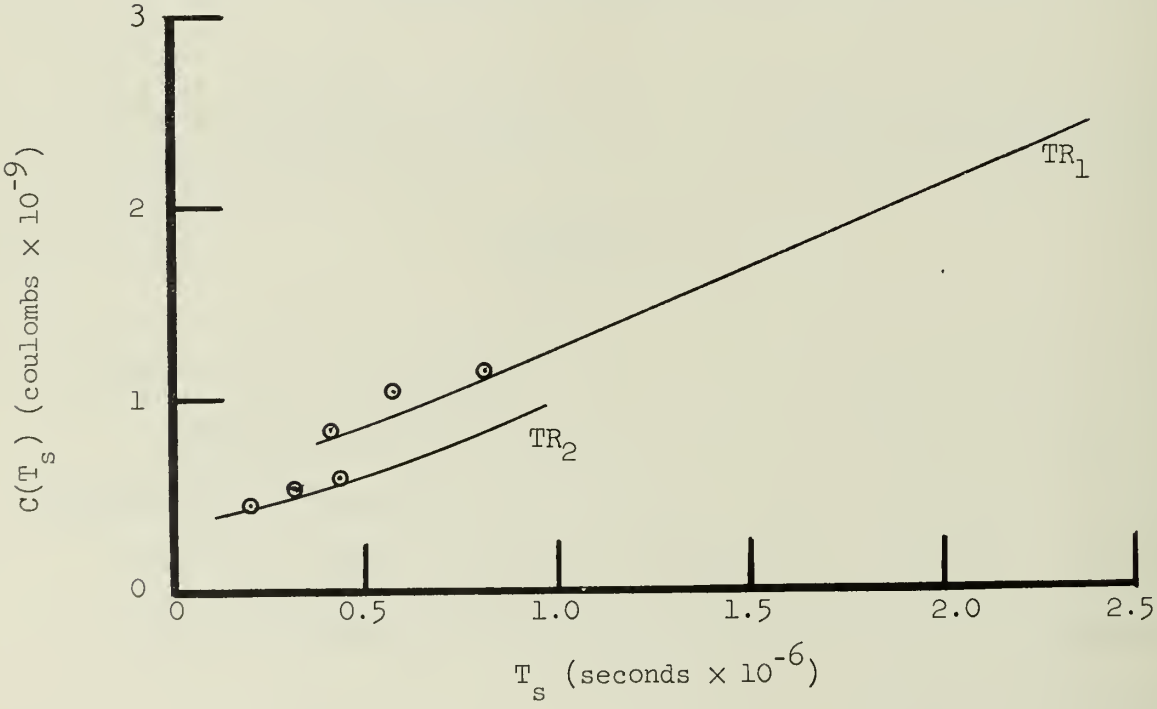

Figure 4.2 Data Points for Exponential Waveforms Compared with C Characteristics for Rectangular Waveforms.

From the curves of Figure 4.1 it is possible to ascertain what combinations of P and g will insure that the transistor enters the active region at some time T, $T < T_s$. Contrary to the case of dc coupling, the fact that the transistor enters the active region along with the fact that $P > 1$, is not sufficient to insure that the transistor will become cut off. If the trigger current is decreasing too quickly, it will permit the transistor to fall back into saturation without ever having reached the cut-off state. This means that there is a possibility that in a bistable circuit such as that of Figure 2.1, $V_3(t)$ would not decrease enough to forward bias Q_2 and initiate regeneration. Some provision must be made to insure that Q_1 will actually cut off.

Let the normalized trigger current be given by Eq. 4.1 and the circuit configuration be that of Figure 3.1. For a fixed g, there exists some minimum value of P, P_{min}, which will drive the transistor into the cut-off region. With each pair (P_{min}, g) there is associated a time T_c equal to the time the transistor enters the cut-off region. The relationship is

$$P_{min} \exp(-gT_c) \cong 1 \qquad 4.5$$

which follows from the fact that as the transistor approaches cut-off, $I_{b1}(t)$ approaches zero and that prior to cut off V_1 is nearly constant. Measured values of $P_{min} \exp(-gT_c)$ ranged from 0.99 to 1.07. Similar reasoning leads to a reformulation of Eq. 4.5 as

$$P \exp(-g_{max} T_c) \cong 1 \qquad 4.6$$

Where g_{max} is the maximum value of g for a fixed P which will permit the transistor to be driven into the cut-off region.

It is apparent that if one could find a functional relationship between two of P, g, and T_c, then specifying one would determine the other two. Data was taken relating 1/g and T_c for TR_1 and TR_2 and is presented in Figure 4.3. From this figure it is possible to choose a design line, DL_2, which is taken to represent the transistor over the operating range. The equation of DL_2 was chosen to be

$$T_c = 2.0 \times 10^{-6} \text{ sec.} + \frac{1}{8g} . \qquad 4.7$$

Solving Eq. 4.5, with the left member equated to 1.1 for safety, and Eq. 4.7 for P_{min} as a function of 1/g gives

$$P_{min} = 1.1 \exp \left[\frac{2}{1/g} + \frac{1}{8} \right] \qquad 4.8$$

A curve displaying the relationship of Eq. 4.8 is presented in Figure 4.4 along with experimental data for TR_1 and TR_2.

$$\lim_{g \to 0} P_{min} = 1.1 \exp(0.125) = 1.25 \qquad 4.9$$

Equation 4.9 predicts that for g = 0, the minimum value of P_{min} which will insure that the transistor enters the cut-off region is 1.25. This is contrary to the value of 1.0 predicted in Part 3 of this report, and indicates that the model may be overly pessimistic for small values of g.

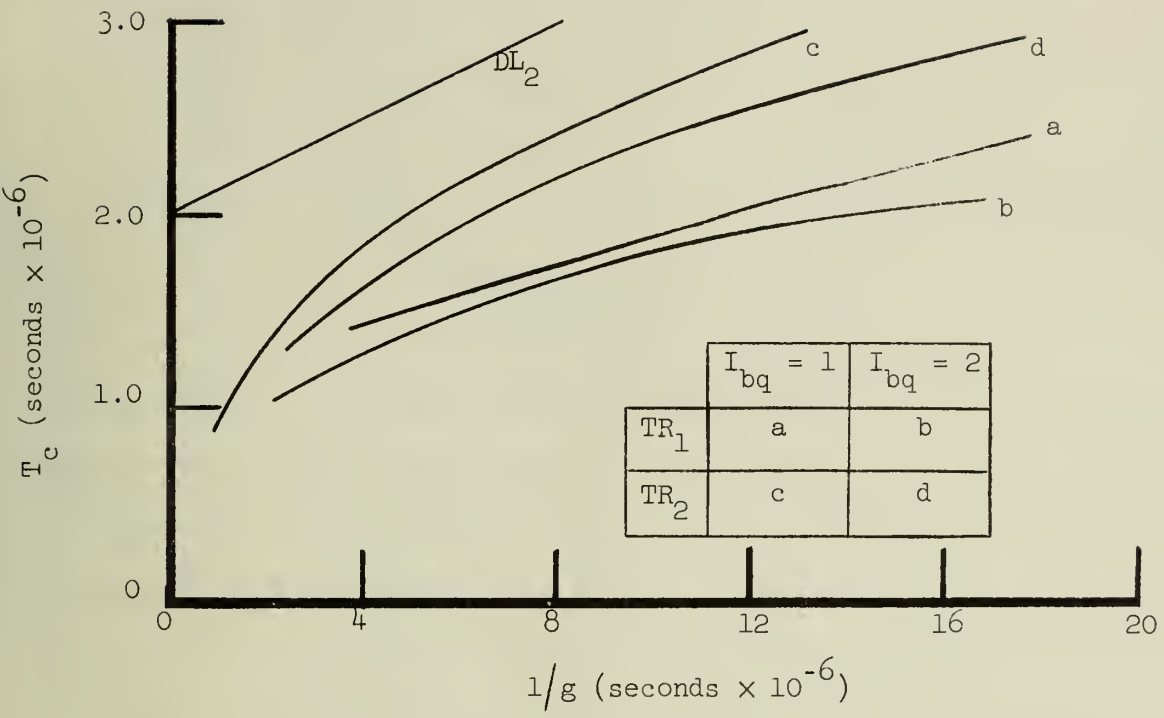

Figure 4.3 Cut-off Time as a function of the Trigger Current Time Constant.

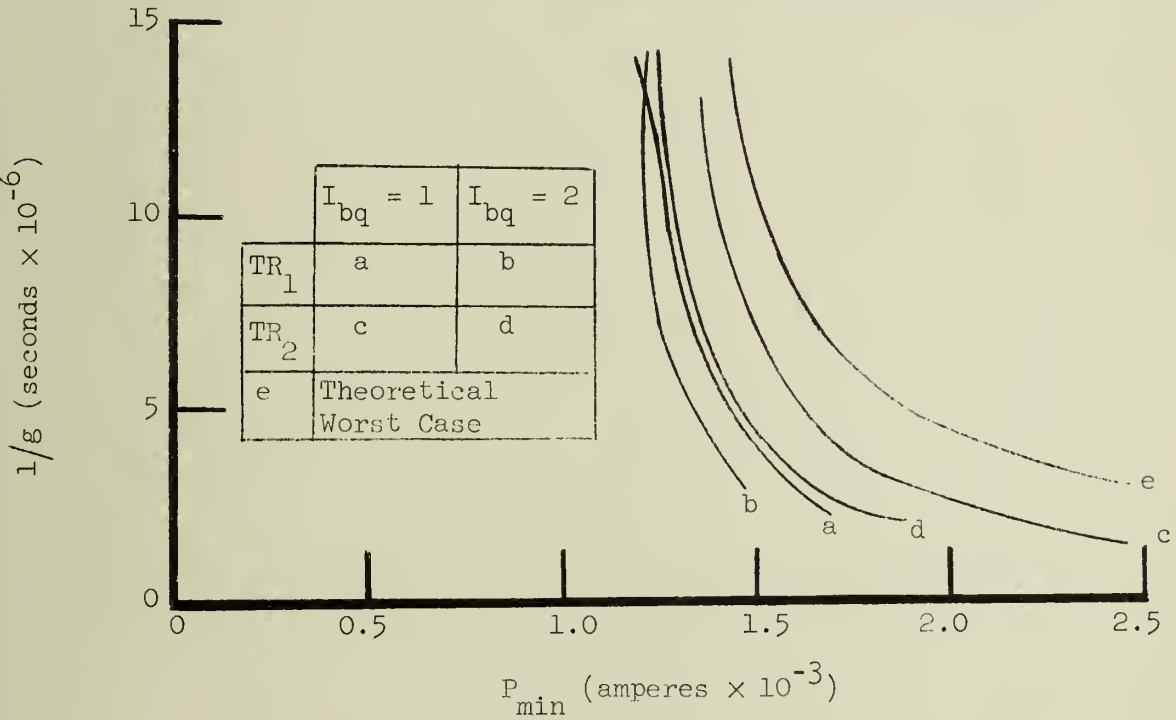

Figure 4.4 Minimum Normalized Pulse Current as a Function of the Trigger Current Time Constant.

Figure 4.5 is a modification of Figure 4.1 which incorporates Eq. 4.8 as a constraint. For a given trigger current time constant, $1/g$, Figure 4.5 presents those values of normalized trigger current, P, which assure that the transistor will enter the cut-off region. In addition, Figure 4.5 places a maximum value on the storage time, T_s.

In summary, Figure 4.4 is the most useful of the curves. It indicates that if P, the ratio of the trigger current to the worst case quiescent base current, equals 1.5, then the trigger current time constant, $1/g$, should be at least 10×10^{-6} seconds. Increasing P to 2.0 permits a decrease in the time constant to 4×10^{-6} seconds. If P is less than 1.5, a very large time constant is called for, while if P is greater than 2.0 a small increase in the time constant will permit a large reduction in P. It thus appears that $1.5 \leq P \leq 2.0$ is a reasonable design target. Over this range the time constant can be represented by:

$$1/g \cong 28 - 12\ P \quad \text{seconds} \times 10^{-6}, \quad 1.5 \leq P \leq 2.0 \qquad 4.10$$

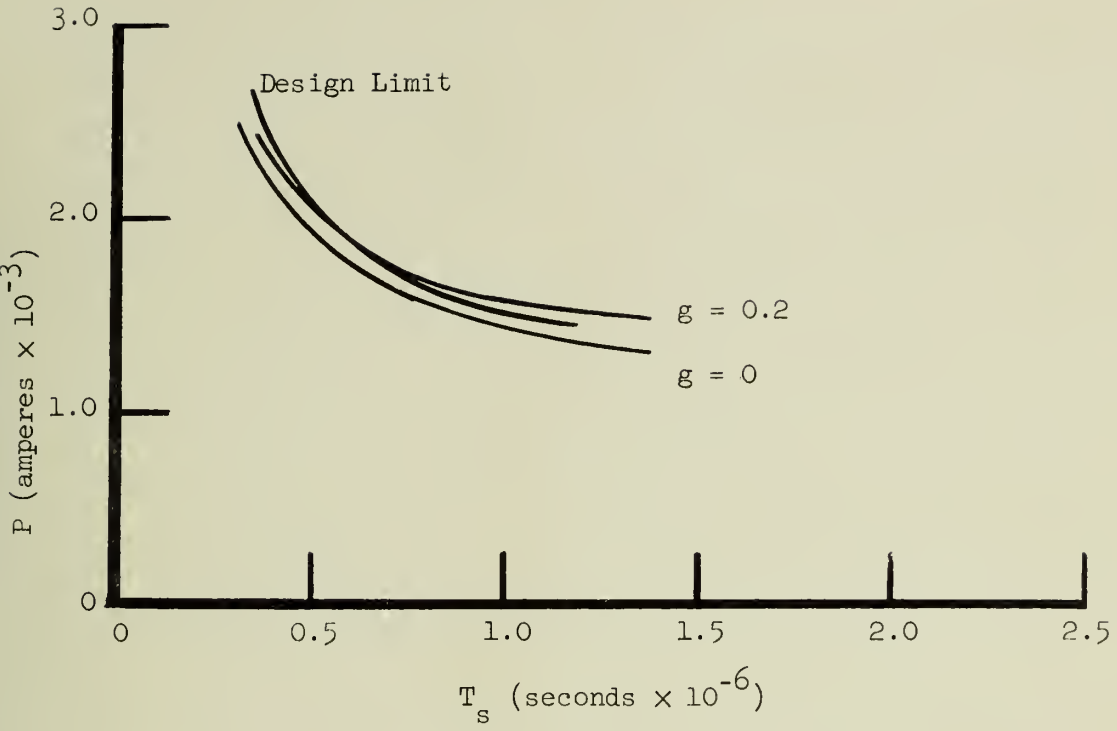

Figure 4.5 Normalized Trigger Current as a Function of T_s and g.

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